APPLICATION NOTE

PAC PCB Layout Guidelines

Power Application Controller™

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PCB LAYOUT GUIDELINES

The PAC52XX family of controllers has a high level of analog integration to make system design much easier for many types of high-voltage control applications. Because of this integration, layout requirements are important for proper operation of the system.

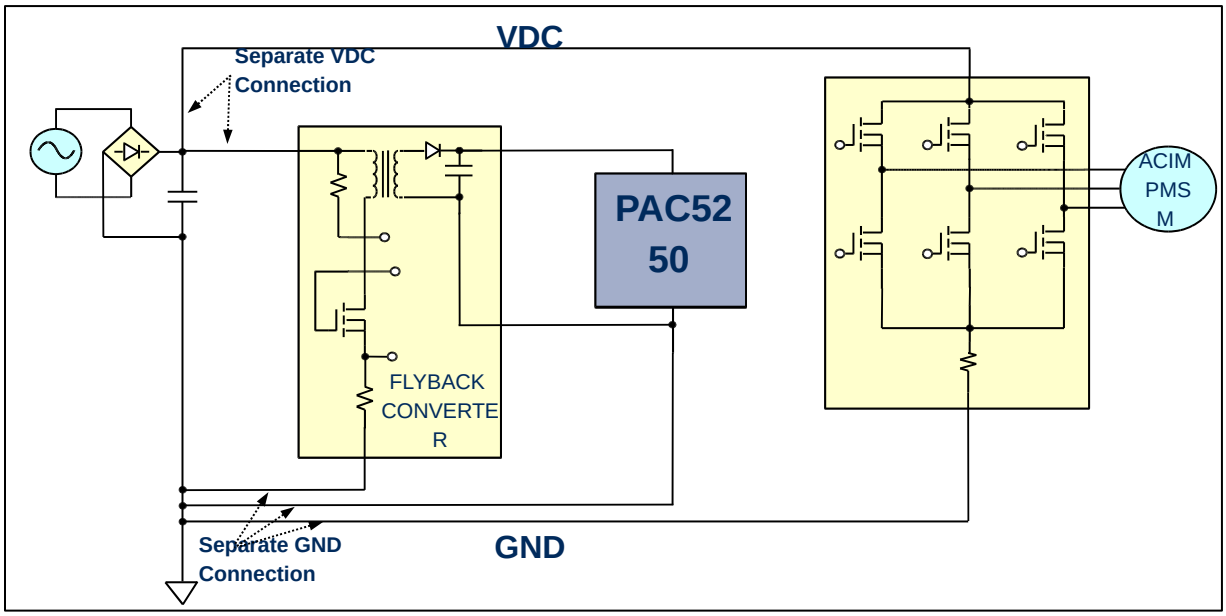
This document provides an overview of the layout guidelines for both high and low-voltage systems using the PAC52XX family of power application controllers.

1. Ground Connections

The ground connection to the IC (IC Ground), the ground connection to the DC-DC (DC-DC Ground), and the ground connection to the motor drive FETs (Power Ground) should be drawn to be isolated from each other. They should only get connected together at the main supply bus capacitor. Please refer to the figure below for illustration.

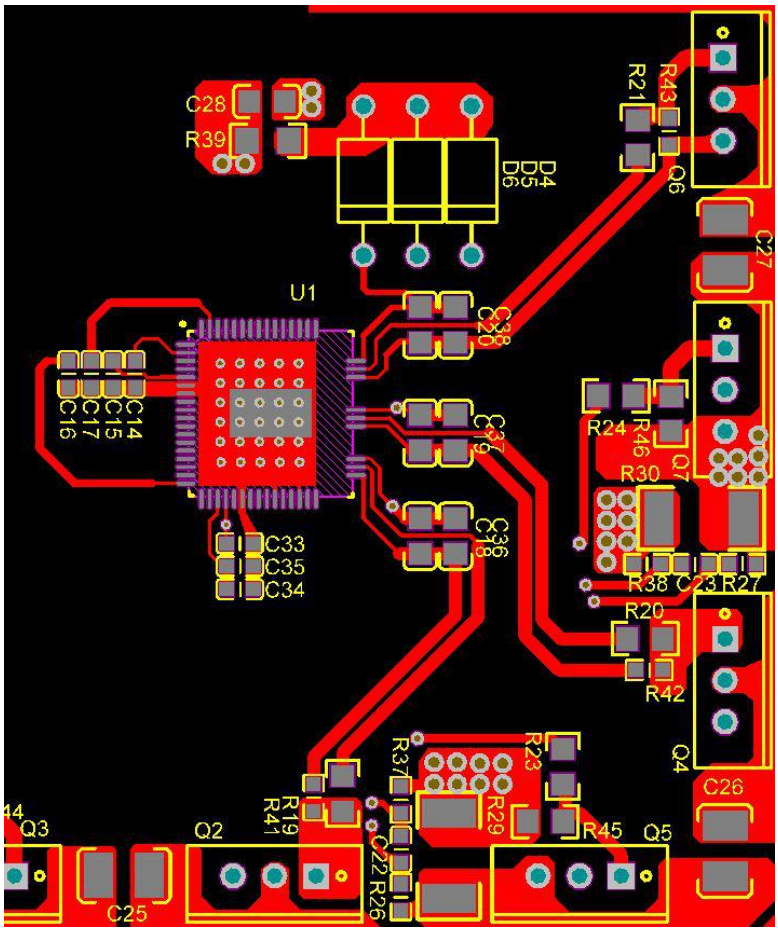
All PAC52XX device ground pins (VSS, VSSA and VSSP), if available in the IC package should be connected directly to the thermal/ground pad at the bottom of the package.

The thermal/ground pad at the bottom of the package should have a solid connection with multiple vias to the IC Ground portion of the ground plane on the PCB.



2. Power Decoupling Capacitors

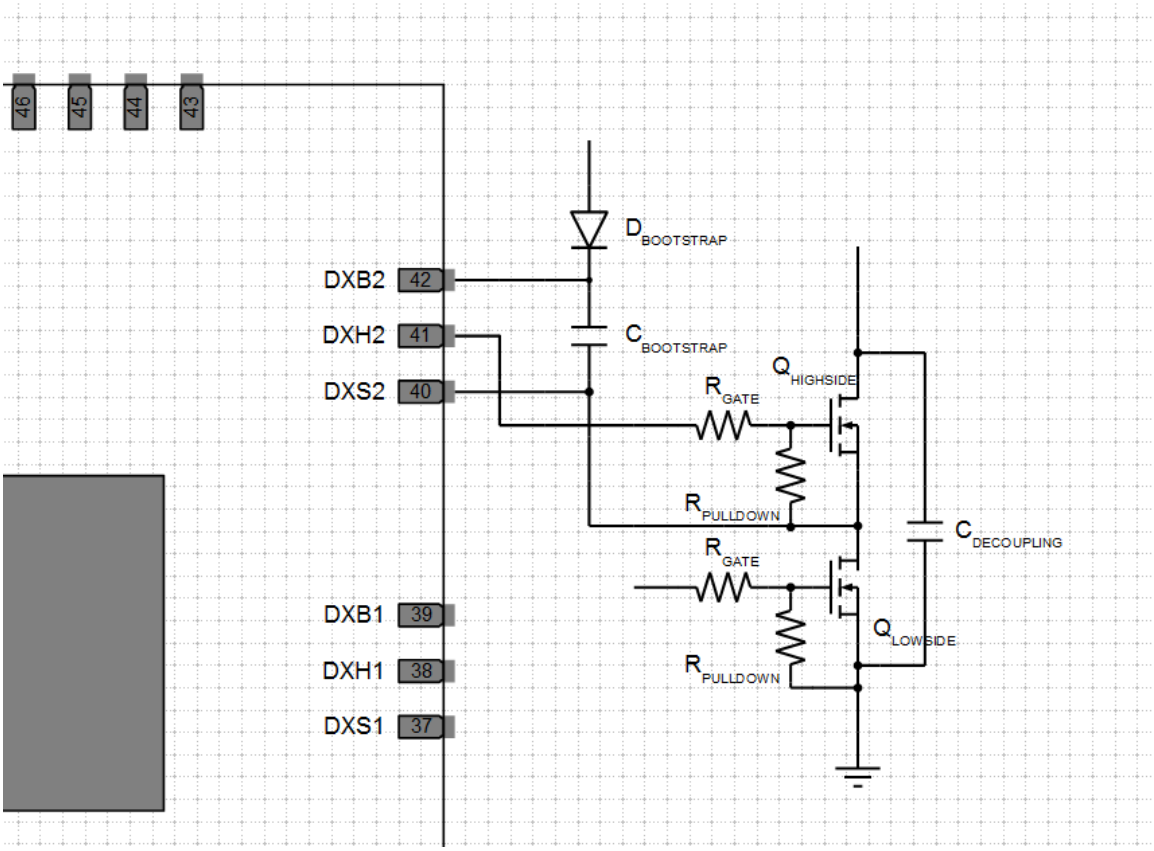
The decoupling capacitors for VCC18, VCC33, VCCIO, VSYS, VHM, CSM should all be placed as close as possible to the device and routed with the shortest traces possible. Please refer to the following designators in the figure below for illustration on the recommended placement of the decoupling capacitors: C14, C15, C16, C17, C33, C34, and C35.



Decoupling Cap Placement & High-Side Driver Routing

3. Gate Drivers

Below are the recommendations to follow for the PCB connection to the gate drivers. Please refer to the figure below for reference.



High-Side Gate Driver Schematic

- The high side driver should be fan out to meet IPC-2221A creeping distance recommendations (high voltage designs only).
- The high-side gate driver bootstrap capacitor $C_{BOOSTRAP}$ and boot-strap diode $D_{BOOSTRAP}$ should be placed as close as possible to the device.
- Both High-Side and Low-Side gate drive resistor R_{GATE} and $R_{PULLDOWN}$ should be placed as close as possible to the Power FET.
- The Half-Bridge decoupling capacitor $C_{DECOUPLING}$ should be placed as close as possible to $Q_{HIGHSIDE}$ and $Q_{LOWSIDE}$

4. ANALOG INPUTS

RC filter or filter capacitors for the AIO analog inputs should be placed as close as possible to the device, with ground routing as short as possible.

ABOUT ACTIVE-SEMI

Active-Semi, Inc. headquartered in Dallas, TX is a leading innovative semiconductor company with proven power management, analog and mixed-signal products for end-applications that require power conversion (AC/DC, DC/DC, DC/AC, PFC, etc.), motor drivers and control and LED drivers and control along with ARM microcontroller for system development.

Active-Semi's latest family of Power Application Controller (PAC)™ ICs offer high-level of integration with 32-bit ARM Cortex M0, along with configurable power management peripherals, configurable analog front-end with high-precision, high-speed data converters, single-ended and differential PGAs, integrated low-voltage and high-voltage gate drives. PAC IC offers unprecedented flexibility and ease in the systems design of various end-applications such as Wireless Power Transmitters, Motor drives, UPS, Solar Inverters and LED lighting, etc. that require a microcontroller, power conversion, analog sensing, high-voltage gate drives, open-drain outputs, analog & digital general purpose IO, as well as support for wired and wireless communication. More information and samples can be obtained from http://www.active-semi.com or by emailing marketing@active-semi.com

Active-Semi shipped its 1 Billionth IC in 2012, and has over 120 in patents awarded and pending approval.